XQR SPACE-GRADE PRODUCT SELECTION GUIDE

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Versal™ XQR Devices – Resources & Packaging

	Device Name	Versal AI Core XQR Series	Versal AI Edge XQR Series
		XQRVC1902-1MSBVSRA2197	XQRVE2302-1MSBSSRA784
AI Engine	AI Engines Tiles	400 (AIE)	34 (AIE-ML)
	AI Engine Data Memory (Mb)	100	17
	AIE-ML Shared Memory (Mb)	-	68
	DSP Engines	1,968	464
Programmable Logic	System Logic Cells (K)	1,968	329
	LUTs	899,840	150,272
	NoC Master / NoC Slave Ports	28	5
	Distributed RAM (Mb)	27	4.6
Memory	Total Block RAM (Mb)	34	5.4
	UltraRAM (Mb)	130	43.6
	Accelerator RAM (Mb)	-	32
	Total PL Memory (Mb)	191	86
	DDR Memory Controllers	4	1
	DDR Bus Width	256	64
Processing System	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48 KB/32 KB L1 Cache w/ECC; 1 MB L2 Cache w/ ECC	
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM w/ECC	
	Memory	256 KB On-Chip Memory w/ECC	
	Gigabit Transceivers	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)	
Serial Transceivers	Gigabit Transceivers	44 GTY (26.5625 Gb/s)	8 GTYP (26.5625 Gb/s)
Integrated Protocol IP	PCIe® w/DMA (CPM)	1 x Gen4x8	-
	PCI Express®	4 x Gen4x8	1 x Gen 4x8
	Multirate Ethernet MAC	4	1
Platform	Platform Management Controller	Boot, Security, Safety, Monitoring, High-Speed Debug, and SEU Mitigation (XilSEM)	
Ruggedized Package	Organic BGA, Sn-Pb Solder Balls	VSRA2197, 45 mm x 45 mm, 0.92 mm pitch	SSRA784, 23 mm x 23 mm, 0.8 mm pitch
I/O	I/O	648 XPIO, 44 HDIO, 78 MIO, 44 GTY	216 XPIO, 22 HDIO, 78 MIO, 8 GTYP

Important: Verify all data in this document with the device data sheets.

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Kintex™ UltraScale™ XQR FPGAs – Resources & Packaging

	Device Name		RT XQRKU060
Logic	System Logic Cells (K)		726
	CLB Flip-Flops (K)		663
	CLB LUTs (K)		331
Memory	Max. Distributed RAM (Kb)		9,180
	Block RAM Blocks		1,080
	Block RAM (Mb)		38
Clocking	Clock Mgmt Tiles (CMTs)		12
Integrated IP	DSP Slices		2,760
	PCIe® Gen1/2/3		3
I/O	I/O DLLs		48
	Max. Single-Ended HP I/Os		520
	Max. Single-Ended HR I/Os		104
	GTH 12.5 Gb/s Transceivers		32
System Monitor	System Monitor		1
Radiation	TID, SEL		100, >80
Reliability	Package, Test		CNA 1509, B-Flow & Y-Flow
Package	Dimensions (mm)	Ball Pitch (mm)	Total HRIO, HPIO GTH 12.5 Gb/s
CNA1509	40x40	1.0	104, 520 32

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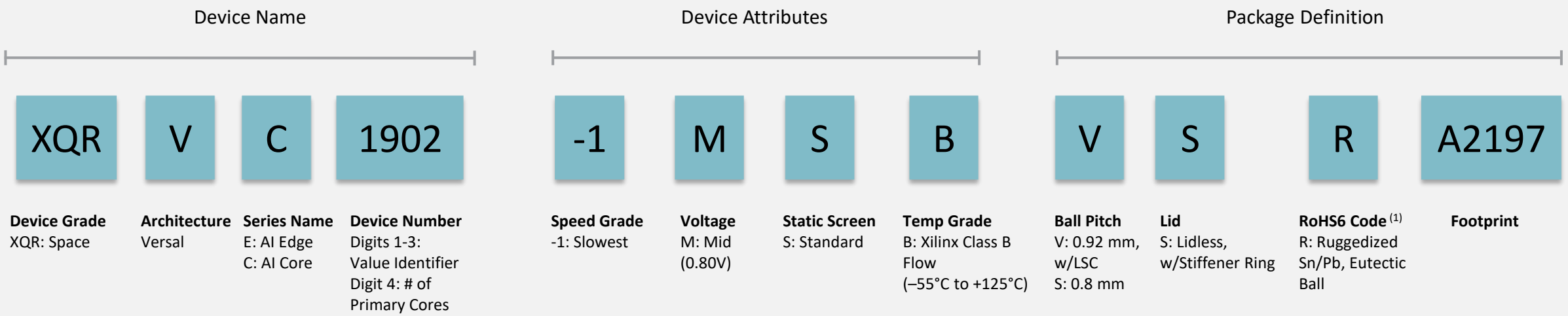
Virtex™ 5 XQR FPGAs – Resources & Packaging

	Device Name	RH XQR5QV
Logic	System Logic Cells	131,072
	CLB Flip-Flops	81,920
Memory	Distributed RAM (Kb)	1,580
	Total Block RAM (Kb)	10,728
Clocking	Digital Clock Manager (DCM)	12
Integrated IP	DSP Slices	320
Phase Lock-Loop	Phase Lock-Loop	6
I/O	GTX Transceivers	18
Embedded Hard IP	10/10/100/1000 EMACs	6
Radiation	TID (krad), SEL (LETs)	1.000, >125
Reliability	Package, Test	B-Flow & V-Flow
Package	**Dimensions (mm)**	**GTX Transceivers, I/O**
CN1752	45x45	18, 836
CF1752	45x45	18, 836

Important: Verify all data in this document with the device data sheets.

Device Ordering Information

Versal™ Adaptive SoCs



Note:

1. All packages have Pb-free bumps.

Device Ordering Information

Kintex™ UltraScale

XQR	K	U	060	-1	CN		A	1509	B

Device Grade
XQR: Space

Family
Kintex

Series Name
UltraScale

Value Index

Speed Grade
-1: Slowest

Package Type
CN: Ceramic Flip-Chip with 1.0 mm Column-grid Array

Footprint Alpha

Package Pin Count

Available Flow:
Y: Xilinx Class Y Flow (-55 to +125°C)
B: Xilinx Class B Flow (-55 to +125°C)

Important: Verify all data in this document with the device data sheets.

Device Ordering Information

Virtex™ 5

XQR	5	V	FX130	-1	CN	1752	V
Device Grade XQR: Space	**Series**	**Family** Virtex	**Value Index**	**Speed Grade** -1: Slowest	**Package Type**[1] CN: Ceramic Flip-Chip with 1.0 mm Column-grid Array	**Nominal Package Pin Count**	**Available Flow:** V: Xilinx V-Grade Flow (-55 to +125°C) B: Xilinx B-Grade Flow (-55 to +125°C)

Note:

1. The CF1752 package is obsolete. Refer to XCN13005, Virtex 4 and Virtex 5 QV FPGA CF Package Assembly Location Change (v2.0, dated 09/22/14) for more information.

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