
XQ DEFENSE-GRADE
PRODUCT SELECTION GUIDE
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AMD Versal™ AI Edge XQ Series Gen 2 – Resources

		XQ2VE3358	XQ2VE3558	XQ2VE3858
AI Engine	AI Engine-ML v2 Tiles	24	96	144
	AIE-ML v2 Data Memory (Mb)	12	48	72
	AIE-ML v2 Shared Memory (Mb)	48	96	288
Processing System	#APU Cores / #RPU Cores	8 / 10	8 / 10	8 / 10
	Application Processing Unit	Arm® Cortex-A78AE, 64 KB I w/ parity & D w/ECC L1 Cache; 512 KB L2 Cache, 1 MB L3 Cache (per 2-core cluster), CMN600 w/4 MB Last-Level Cache (shared)		
	Real-Time Processing Unit	Arm Cortex-R52, 32 KB L1 Cache w/ECC, 128 KB TCM w/ECC		
	Memory	2MB On-Chip Memory w/ECC		
	High-Speed Connectivity	PCI Express® Gen5 x4, USB 3.2, DisplayPort™ 1.4, 10G Ethernet, 1G Ethernet, UFS 3.1		
	General Connectivity	CAN/CAN-FD, SPI, UART, USB 2.0, I2C/I3C, GPIO		
Programmable Logic	System Logic Cells	206,920	492,188	1,188,040
	LUTs	94,592	225,000	543,104
	DSP Engines	184	700	2,064
	NoC Master / NoC Slave Ports	4	7	24
	Distributed RAM (Mb)	2.9	6.9	16.6
Memory	Total Block RAM (Mb)	5.0	13.6	47.2
	UltraRAM (Mb)	13.2	3.4	33.2
	Total PL Memory (Mb)	21.1	23.9	97.0
	DDR Memory Controllers	3	4	5
	DDR Bus Width	96	128	160
Video and Imaging IP	GPU (4-core Arm Mali™-G78AE)	1	1	1
	Video Codec Unit (VCU)	1	1	1
	Image Signal Processor	1	3	3
Transceivers	GTYP (PL Only)	4	12	20
	PS-Dedicated Transceivers	4 x GTYP, 4 x GTR	4 x GTYP, 4 x GTR	4 x GTYP, 4 x GTR
Integrated Connectivity IP	PCI Express® (PLPCIE5)	1 x Gen5 x4	3 x Gen5 x4	4 x Gen5 x 4
	100G Multirate Ethernet MAC	1	1	3
Ordering Information	Military Temp	-1MSM		
	Industrial Temp[1]	-1LSI, -1MSI, -2MSI		

1. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

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AMD Versal™ AI Edge XQ Series Gen 2 – Packaging

			XQ2VE3358	XQ2VE3558	XQ2VE3858
Package	Package Dimensions (mm)	Ball Pitch (mm)	X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTYP (PL Only), GTYP (PS Only)		
SBRA1440	31 x 31	0.8	168, 64, 32 44, 78 4, 4	192, 136, 0 88, 78 4, 4	
SSRA2112	37.5x37.5	0.8		232, 152, 0 44, 78 12, 4	208, 272, 32 44, 78 20, 4
SSRA2397	40 x 40	0.8			208, 272, 32 44, 78 20, 4, 4

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		XQVE2102	XQVE2302
AI Engine	AI Engine-ML Tiles	12	34
	AI Engine Tiles	0	0
	AIE/AIE-ML Data Memory (Mb)	6	17
	AIE-ML Shared Memory (Mb)	48	68
Programmable Logic	System Logic Cells	80,080	328,720
	LUTs	36,608	150,272
	DSP Engines	176	464
	NoC Master / NoC Slave Ports	2	5
	Distributed RAM (Mb)	1.1	4.6
Memory	Total Block RAM (Mb)	1.7	5.4
	UltraRAM (Mb)	13.2	43.6
	Accelerator RAM (Mb)	32	32
	Total PL Memory (Mb)	48	85.6
	DDR Memory Controllers	1	1
	DDR Bus Width	64	64
Processing System	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC	
	Real-Time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC	
	Memory	256KB On-Chip Memory w/ECC	
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)	
Serial Transceivers	GTY Transceivers	0	0
	GTYP Transceivers	0	8
Integrated Protocol IP	PCI Express® (PL PCIE4)	-	1 x Gen4x8
	40G Multirate Ethernet MAC	0	1
Platform	Video Decoder Engines (VDEs)	–	–
	Platform Mgmt Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug	
Ordering Information	Military Temp	-1MSM	
	Industrial Temp(1)	-1LSI, -1MSI, -2MSI	

1. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

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AMD Versal™ AI Edge XQ Series – Packaging

			XQVE2102	XQVE2302
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTY, GTYP	
SBRA484	19x19	0.8	108, 0, 54 0, 78 0, 0	
SSRA784	23x23	0.8	132, 30, 54 0, 78 0, 0	132, 30, 54 22, 78 0, 8

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		XQVC1702	XQVC1902
AI Engine	AI Engines Tiles	304	400
	AI Engine-ML Tiles	0	0
	AI Engine Data Memory (Mb)	76	100
	AIE-ML Shared Memory (Mb)	0	0
Programmable Logic	System Logic Cells (K)	981	1,968
	LUTs	448,512	899,840
	DSP Engines	1,312	1,968
	NoC Master / NoC Slave Ports	21	28
	Distributed RAM (Mb)	14	27
Memory	Total Block RAM (Mb)	34	34
	UltraRAM (Mb)	130	130
	Accelerator RAM (Mb)	0	0
	Total PL Memory (Mb)	178	191
	DDR Memory Controllers	3	4
	DDR Bus Width	192	256
Processing System	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC	
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM w/ECC	
	Memory	256 KB On-Chip Memory w/ECC	
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)	
Serial Transceivers	GTY Transceivers	44	44
	GTYP Transceivers	0	0
Integrated Protocol IP	PCIe® w/DMA (CPM)	1 x Gen4x16	1 x Gen4x16
	PCI Express®	4 x Gen4x8	4 x Gen4x8
	100G Multirate Ethernet MAC	4	4
Platform	Video Decoder Engines (VDEs)	–	–
	Platform Management Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug	
Ordering Information	Military Temp	-1MSM	
	Industrial Temp(1)	-1LSI, -1MSI, -2MSI	

1. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

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AMD Versal™ AI Core XQ Series – Packaging

			XQVC1702	XQVC1902
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTY, GTYP	
NSRG1369	35x35	0.92	132, 246, 0 44, 78 24, 0	
VSRA1596	37.5x37.5	0.92	132, 246, 0 44, 78 32, 0	
VIRA1596	40x40	0.92		132, 246, 0 44, 78 32, 0
VSRD1760	40x40	0.92		186, 426, 0 0, 78 24, 0
VSRA2197	45x45	0.92	192, 294, 0 44, 78 44, 0	186, 462, 0 44, 78 44, 0

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AMD Versal™ Prime XQ Series Gen 2 – Resources

			XQ2VM3358	XQ2VM3558	XQ2VM3858
Processing System	# Application Cores / #Real-Time Cores		8 / 10		
	Application Core Type		Arm® Cortex®-A78AE, 64 KB I w/ parity & D w/ECC L1 Cache; 512 KB L2 Cache		
	Real-Time Core Type		Arm Cortex-R52, 32 KB L1 Cache w/ECC, 128 KB TCM w/ECC		
	High-Speed Connectivity		PCI Express® Gen5 x4[1], USB 3.2, DisplayPort™ 1.4, 10G Ethernet, 1G Ethernet, UFS 3.1		
	General Connectivity		CAN/CAN-FD, SPI, UART, USB 2.0, I2C/I3C, GPIO		
	Application Cores	Cores Per Cluster / #Clusters	2 / 4		
		L3 Cache Per Cluster (MB)	1		
		System-Level Cache (MB)	4		
	Real-Time Cores	Cores Per Cluster / #Clusters	2 / 5		
	On-Chip Memory w/ ECC (MB)		2		
Programmable Logic	System Logic Cells		206,920	492,188	1,188,040
	LUTs		94,592	225,000	543,104
	DSP Engines		184	700	2,064
	NoC Master / NoC Slave Ports		4	7	24
	Distributed RAM (Mb)		2.9	6.9	16.6
Memory	Block RAM (Mb)		4.9	13.6	47.2
	UltraRAM (Mb)		13.2	3.4	33.2
	Total PL Memory (Mb)		21.1	23.9	97.0
	32b DDR5 Memory Controllers (DDRMC5E)		3	4	5
	DDR Bus Width		96	128	160
Video and Imaging IP	GPU (4-core Arm Mali™-G78AE)		4	4	4
	Video Codec Unit (VCU)		1	1	1
Transceivers	GTYP (PL Only)		4	12	20
	PS-Dedicated Transceivers[2]		4 x GTYP, 4 x GTR	4 x GTYP, 4 x GTR	4 x GTYP, 4 x GTR
Integrated Connectivity IP	PCI Express® (PLPCIE5)		1 x Gen5 x4	3 x Gen5 x4	4 x Gen5 x4
	100G Multirate Ethernet MAC		1	1	3
Ordering Information	Military Temp		-1MSM		
	Industrial Temp[3]		-1LSI, -1MSI, -2MSI		

1. PS-Dedicated PCIe Gen 5 support is provided by the MDB5 hard IP block.
2. PS-Dedicated transceivers connectivity: GTYP: 10G Ethernet, PCI Express, and HSDP; GTR: USB and DisplayPort.
3. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

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			XQ2VE3354	XQ2VE3554	XQ2VE3858
Package	Package Dimensions (mm)	Ball Pitch (mm)	X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTYP (PL Only), GTYP (PS Only)		
SBRA1440	31 x 31	0.8	168, 64, 32 44, 78 4, 4, 4	192, 136, 0 88, 78 4, 4, 4	
SSRA2112	37.5x37.5	0.8		232, 152, 0 44, 78 12, 4, 4	208, 272, 32 44, 78 20, 4, 4

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AMD Versal™ Prime XQ Series – Resources

		VM1102	VM1402	VM1502	VM1802
Programmable Logic	System Logic Cells (K)	329	1,238	981	1,968
	LUTs	150,272	565,760	448,512	899,840
	DSP Engines	464	1,696	1,312	1,968
	NoC Master / NoC Slave Ports	5	18	21	28
	Distributed RAM (Mb)	5	17	14	27
Memory	Total Block RAM (Mb)	5	40	34	34
	Total UltraRAM (Mb)	44	80	130	130
	Total PL Memory (Mb)	54	137	178	191
	DDR4 Memory Controllers	1	4	3	4
	DDR5 Memory Controllers	-	-	-	-
	DDR Bus Widths	64	256	192	256
Processing System	Application Processing Unit	Dual-core Arm® Cortex-A72, 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC			
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM w/ECC			
	Memory	256 KB On-Chip Memory w/ECC			
	Connectivity	Ethernet (x2); USB 2.0 (x1); UART (x2); SPI (x2); I2C (x2); CAN-FD (x2)			
Serial Transceivers	GTY Transceivers	0	24	44	44
	GTYP Transceivers	8	0	0	0
	GTM Transceivers (58G[1] (112G))	0	0	0	0
Integrated Protocol IP	PCIe® w/DMA (CPM4)	-	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16
	PCIe® (PL PCIE4)	-	2 x Gen4x8	4 x Gen4x8	4 x Gen4x8
	PCIe (PL PCIE5)	1 x Gen4x8			
	100G Multirate Ethernet MAC	1	2	4	4
	600G Ethernet MAC	-	-	-	-
	400G High Speed Crypto	-	-	-	-
Ordering Information	Military Temp	-1MSM			
	Industrial Temp[2]	-1MSI, -1LSI, -2MSI			

1. 58G supported only in -3 speedgrade. For devices supporting up to -2 speedgrade, the maximum GT speed is 56G.
2. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

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AMD Versal™ Prime XQ Series – Packaging

			VM1102	VM1402	VM1502	VM1802
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTY, GTYP, GTM (112G)			
SSRA784	23x23	0.8	132, 30, 54 22, 78 0, 8, 0			
VSRC1596	37.5x37.5	0.92		168, 480, 0 22, 78 24, 0, 0		
VSRD1760(1)	40x40	0.92		168, 480, 0 0, 78 16, 0, 0		186, 462, 0 0, 78 24, 0, 0
VSRA2197	45x45	0.92			192, 294, 0 44, 78 44, 0, 0	186, 462, 0 44, 78 44, 0, 0

1. VM1402 in VSRD1760 supports peak LPDDR4 in 324 I/O only. The remaining 324 I/O support limited data rates. See the associated data sheet.

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		XQ2VP3202	XQ2VP3602
Programmable Logic	System Logic Cells	1,743,560	3,273,480
	LUTs	797,056	1,496,448
	DSP Engines	4,004	7,616
	NoC Master / NoC Slave Ports	24	40
	Distributed RAM (Mb)	24	46
Memory	Total Block RAM (Mb)	53	99
	UltraRAM (Mb)	101	182
	Total PL Memory (Mb)	178	327
	DDR Memory Controllers	4	8
	Total DDR Bus Width	128	256
Processing System	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC	
	Real-Time Processing Unit	Dual-core Arm cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM w/ ECC	
	Memory	256 KB On-Chip Memory w/ ECC	
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)	
Integrated Protocol IP	PCIe (PL PCIE5)	1x Gen5x4	1 x Gen5x4
	PCIe® w/ DMA & CXL® 3.1 (CPM6)	2x Gen6x8	2x Gen6x8
	GTM2 Transceivers	32	72
	100G Multirate Ethernet MAC	2	1
	600G Ethernet MAC	2	5
	High-Speed Crypto Engines	2	1
	LDPC Decoder	6	0
Ordering Information	Military Temp	-1MSM	
	Industrial Temp[1]	-1LSI, -1MSI, -2MSI	

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			XQ2VP3202	XQ2VP3602
Package	Package Dimensions (mm)	Ball Pitch (mm)	X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTM2 PL Only 56G (112G),[1][2] GTM2 CPM6 32G (64G)[2][3]	
NSRO1369	35 x 35	0.92	104, 224, 0 22, 52 24 (12), 8 (4)	
VSRJ1760	40 x 40	0.92	136, 248, 32 22, 78 16 (12), 16 (16)	
VSRA3014	58.5 x 46.5	0.92		136, 544, 32 0, 78 48 (24), 16 (16)
VSRC3340	55 x 55	0.92		104, 600, 32 0, 78 56 (56), 16 (16)

1. For 128G data rate support, contact your local AMD sales representative.
2. All GTM2 PL Only can operate at 56G; the quantity that can operate up to 112G is shown in parentheses. All GTM2 CPM can operate at 32G; the quantity that can operate up to 64G is shown in parentheses.
3. GTM2 transceivers connected to CPM6 can also bypass CPM6 (using the GT Direct mode) and access PL to support select non-PCIe protocols up to 32G NRZ (in -3 speedgrade) or 25G NRZ (in -2 speedgrade).

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AMD Versal™ Premium XQ Series – Resources

		XQVP1052	XQVP1202	XQVP1402	XQVP1502	XQVP2502	XQVP1702
AI Engine	AI Engines Tiles	-	-	-	-	472	-
	AI Engine Data Memory (Mb)	-	-	-	-	118	-
Programmable Logic	System Logic Cells (K)	1,186	1,969	2,233	3,763	3,738	5,558
	LUTs	542,080	900,224	1,020,928	1,720,448	1,708,672	2,540,672
	DSP Engines	1,572	3,984	2,672	7,440	7,392	10,896
	NoC Master / NoC Slave Ports	22	28	42	52	52	76
	Super Logic Regions (SLRs)(1)	-	-	-	2	2	3
	Distributed RAM (Mb)	17	27	31	53	52	78
Memory	Block RAM (Mb)	26	47	70	89	89	132
	UltraRAM (Mb)	138	190	181	366	366	541
	Multiport RAM (Mb)	80	-	-	-	-	-
	Total PL Memory (Mb)	261	264	282	508	507	751
	DDR Memory Controllers	2	4	3	4	4	4
	DDR Bus Width	128	256	192	256	256	256
Processing System	APU	Dual-core Arm® Cortex®-A72, 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC					
	RPU	Dual-core Arm Cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM w/ECC					
	Memory	256 KB On-Chip Memory w/ECC					
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)					
Serial Transceivers	GTY Transceivers	8	-	-	-	-	-
	GTYP Transceivers	-	28(2)	8	28(2)	28(2)	28(2)
	GTM Transceivers (58G (112G))	36 (18)	20 (10)	96 (64)(3)	60 (30)	60 (30)	100 (50)
Integrated Protocol IP	PCIe® w/DMA (CPM4)	2 x Gen4x4	-	-	-	-	-
	PCIe w/DMA (CPM5)	-	2 x Gen5x8	-	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8
	PCIe (PL PCIE4)	1 x Gen4x8	-	-	-	-	-
	PCIe (PL PCIE5)	-	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4
	100G Multirate Ethernet MAC	5	2	6	4	4	6
	600G Ethernet MAC	3	1	11	3	3	5
	600G Interlaken	2	-	-	1	1	2
	400G High-Speed Crypto Engine	1	1	4	2	2	3
Ordering Information	Military	-1MSM			-	-	-
	Industrial(3)	-1LSI, -1MSI, -2MSI					

1. Refers to logic SLRs only.
2. 16 GTYP transceivers are dedicated to the CPM5 for PCI Express use.
3. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

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AMD Versal™ Premium XQ Series – Packaging

			XQVP1052	XQVP1202	XQVP1402	XQVP1502	XQVP2502	XQVP1702
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, DDR+PL, PL Only HDIO, MIO GTY, GTM (112G)	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTYP, GTM (112G)				
SBRJ1369	31x31	0.8	192, 132, 0 0, 78 8, 16 (8)					
VSRA2785	50x50	0.92		132, 516, 54 0, 78 28, 20 (10)	180, 306, 0 44, 78 8, 80 (40)	132, 516, 54 0, 78 28, 56 (28)		
VSRA3340	55x55	0.92			180, 306, 0 44, 78 8, 96 (48)	132, 354, 0 0, 78 28, 60 (30)		132, 354, 0 0, 78 28, 88 (44)
VSRB3340	55x55	0.92					132, 516, 54 0, 78 28, 60 (30)	

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AMD Versal™ RF XQ Series – Resources

			XQVR1602	XQVR1652	XQVR1902	XQVR1952
RF	14-bit RF-ADC	# of ADCs	16	4	16	8
		Max Rate (GSPS)	8	32	8	32
	14-bit RF-DAC	# DACs	16	8	16	16
		Max Rate (GSPS)	16	16	16	16
	LDPC Decoder		4	4	6	6
	1 GSPS Channelizer		224	224	96	96
	FFT/iFFT		28	28	36	36
	Poly Block		-	-	24(1)	24(1)
AI Engine	AI Engine (AIE) Tiles		126	126	120	120
	AIE Data Memory (Mb)		32	32	30	30
Programmable Logic	System Logic Cells		1,205,400	1,205,400	2,473,800	2,473,800
	LUTs		551,040	551,040	1,130,880	1,130,880
	DSP Engines		2,256	2,256	3,976	3,976
	NoC Master / NoC Slave Ports		16	16	36	36
	Distributed RAM (Mb)		17	17	35	35
Memory	Total Block RAM (Mb)		39	39	80	80
	UltraRAM (Mb)		100	100	74	74
	Total PL Memory (Mb)		156	156	189	189
	DDR Memory Controllers (DDRMC5e)		5	5	5	5
	DDR Bus Width		160	160	160	160
Processing System	Application Processing Unit		Dual-core Arm® Cortex-A72, 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC			
	Real-Time Processing Unit		Dual-core Arm Cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM w/ ECC			
	Memory		256 KB On-Chip Memory w/ ECC			
	Connectivity		Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)			
Serial Transceivers	GTYP Transceivers		12	12	-	-
	GTM Transceivers (56G (112G))		8 (4)	8 (4)	-	-
	GTM2 Transceivers (56G (112G))		-	-	20 (10)	20 (10)
Integrated Protocol IP	PCIe® (PLS PCIE5)		1 x Gen5x4	1 x Gen5x4	1 x Gen5x4	1 x Gen5x4
	100G Multirate Ethernet MAC		2	2	2	2
	600G Ethernet MAC		-	-	3	3
Platform	Platform Mgmt Controller		Boot, Security, Safety, Monitoring, and High-Speed Debug			
Ordering Information	Military Temp[2]		-1MSM			
	Industrial Temp[2]		-1LSI, -1MSI, -2MSI			

1. Each poly block can be also configured as 16 channelizers. Two poly blocks can be combined to form an arbitrary resampler.
2. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

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AMD Versal™ RF XQ Series – Packaging

			XQVR1602	XQVR1652	XQVR1902	XQVR1952
Package	Package Dimensions (mm)	Ball Pitch (mm)	X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTYP, GTM (112G) RF-ADC (8G), RF-ADC (32G), RF-DAC (16G)		X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTM2 (112G) RF-ADC (8G), RF-ADC (32G), RF-DAC (16G)	
VSRG1596	37.5 X 37.5	0.92	144, 208, 0 22, 78 4, 4 (2) 12, 0, 8	144, 208, 0 22, 78 4, 4 (2) 0, 4, 8		
VSRA2488	47.5 x 47.5	0.92	144, 304, 0 22, 78 12, 8 (4) 16, 0, 16	144, 304, 0 22, 78 12, 8 (4) 0, 4, 8	144, 304, 0 22, 78 20 (10) 16, 0, 16	144, 304, 0 22, 78 20 (10) 0, 8, 16

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AMD Zynq™ UltraScale+™ XQ RFSoC Resources

	Device Name		XQZU21DR	XQZU28DR	XQZU29DR	XQZU48DR	XQZU49DR	XQZU65DR	XQZU67DR	
				Gen 1		Gen 3		DFE		
PS			**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.3 GHz, **Dual-core** Arm Cortex-R5F MPCore up to 533 MHz							
RF Data Converter	12-bit RF-ADC w/DDC	# of ADCs	0	8	16	–	–	–	–	
		Max Rate (GSPS)	0	4.096	2.058	–	–	–	–	
	14-bit RF-ADC w/DDC	# of ADCs	–	–	–	8	16	6	8	2
		Max Rate (GSPS)	–	–	–	5.0	2.5	5.9	2.95	5.9
	14-bit RF-DAC w/DUC	# of DACs	0	8	16	8	16	6	8	
		Max Rate (GSPS)	0	6.554	6.554	9.85[3]	9.85[3]	10.0[4]	10.0[4]	
	SD-FEC		8	8	0	8	0	0	0	
	Digital Front-End (DFE)		–	–	–	–	–	✓	✓	
	Number of DDCs per RF-ADC[1]		0	1	1	1	1	1	1	
	RF input Freq max. GHz		4					7.125		
	Decimation / Interpolation		1x, 2x, 4x, 8x			1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x				
Programmable Logic (PL)	System Logic Cells (K)		930	930	930	930	930	489	489	
	CLB LUTs (K)		425	425	425	425	425	224	224	
	Max. Dist. RAM (Mb)		13.0	13.0	13.0	13.0	13.0	6.8	6.8	
	Total Block RAM (Mb)		38.0	38.0	38.0	38.0	38.0	22.8	22.8	
	UltraRAM (Mb)		22.5	22.5	22.5	22.5	22.5	45.0	45.0	
	DSP Slices		4,272	4,272	4,272	4,272	4,272	1,872	1,872	
	GTY Transceivers		16	16	16	16	16	8	8	
	PCIe® Gen3 x16		2	2	2	–	–	–	–	
	PCIeGen3 x16/Gen4 x8 / CCIX[2]		–	–	–	2	2	0	0	
	150G Interlaken		1	1	1	1	1	0	0	
	100G Ethernet MAC/PCS w/RS-FEC		2	2	2	2	2	1	1	
	System Monitor		2	2	2	2	2	2	2	
	Speed Grades		-1I, -1LI, -1M -2I	-1I, -1LI, -1M -2I	-1I, -1LI, -1M -2I	-1I, -1LI, -1M -2I, -2LI	-1I, -1LI, -1M -2I, -2LI	-1I, -1LI, -1M -2I, -2LI	-1I, -1LI, -1M -2I, -2LI	

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AMD Zynq™ UltraScale+™ XQ RFSoC Packaging

PS I/Os(1), High-Density (HD) I/O, High-Performance (HP) I/Os
PS-GTR, GTY, RF-ADC, RF-DAC

Package(2)	Dimensions (mm)	Ball Pitch (mm)	XQZU21DR	XQZU28DR	XQZU29DR	XQZU48DR	XQZU49DR	XQZU65DR	XQZU67DR
			Gen 1			Gen 3		DFE	
FFRD1156	35x35	1.0	214, 72, 208 4, 16, 0, 0						
FFRE1156	35x35	1.0		214, 48, 104 4, 8, 8, 8		214, 48, 104 4, 8, 8, 8		214, 24, 130 4, 8, 6, 6	214, 24, 130 4, 8, 10, 8
FFRG1517	40x40	1.0		214, 48, 299 4, 16, 8, 8					
FSRG1517	40x40	1.0				214, 48, 299 4, 16, 8, 8			
FFRF1760	42.5x42.5	1.0			214, 96, 312 4, 16, 16, 16				
FSRF1760	42.5x42.5	1.0					214, 96, 312 4, 16, 16, 16		

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. For full part number details, see the Ordering Information section in DS895, *XQ UltraScale Architecture Data Sheet: Overview*.

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AMD Zynq™ UltraScale+™ XQ MPSoC Resources

		Device Name	XQZU3EG	XQZU5EV	XQZU7EV	XQZU9EG	XQZU11EG	XQZU15EG	XQZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** Arm® Cortex™-A53 MPCore™ up to 1.33 GHz						
		Memory w/ECC	L1 Cache 32 KB I / D per core, L2 Cache 1 MB, on-chip Memory 256 KB						
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5F MPCore™ up to 533 MHz						
		Memory w/ECC	L1 Cache 32 KB I / D per core, Tightly Coupled Memory 128 KB per core						
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 600 MHz						
		Memory	L2 Cache 64 KB						
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC						
		Static Memory Interfaces	NAND, 2x Quad-SPI						
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort™, 4x Tri-mode Gigabit Ethernet						
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains						
		Security	RSA, AES, and SHA						
		AMS - System Monitor	10-bit, 1MSPS - Temperature, Voltage, and Current Monitor						
		PS to PL Interface	12 x 32/64/128b AXI Ports						
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	154	256	504	600	653	747	1,143
		CLB Flip-Flops (K)	141	234	461	548	597	682	1,045
		CLB LUTs (K)	71	117	230	274	299	341	523
	Memory	Max. Distributed RAM (Mb)	1.8	3.5	6.2	8.8	9.1	11.3	9.8
		Total Block RAM (Mb)	7.6	5.1	11.0	32.1	21.1	26.2	34.6
		UltraRAM (Mb)	-	18.0	27.0	-	22.5	31.5	36.0
	Clocking	Clock Management Tiles (CMTs)	3	4	8	4	8	4	11
	Integrated IP	DSP Slices	360	1,248	1,728	2,520	2,928	3,528	1,968
		Video Codec Unit (VCU)	-	1	1	-	-	-	-
		PCI Express® Gen 3x16	-	2	2	-	4	-	5
		150G Interlaken	-	-	-	-	1	-	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	2	-	4
		AMS - System Monitor	1	1	1	1	1	1	1
	Transceivers	GTH 16.3 Gb/s Transceivers	-	16	24	24	32	24	44
		GTY 28.2 Gb/s Transceivers	-	-	-	-	16	-	28
	Speed Grades	M-Temperature	-1						
		I-Temperature	-1 -1L -2						

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AMD Zynq™ UltraScale+™ XQ MPSoC Packaging

PSIO(1), HDIO, HPIO

PS-GTR 6 Gb/s, GTH 16.3 Gb/s, GTY 28.2 Gb/s

Package(2,3)	Dimensions (mm)	Ball Pitch (mm)	XQZU3EG	XQZU5EV	XQZU7EV	XQZU9EG	XQZU11EG	XQZU15EG	XQZU19EG
SFRA484(4)	19x19	0.8	170, 24, 58 4, 0, 0						
SFRC784(4,5)	23x23	0.8	214, 96, 156 4, 0, 0	214, 96, 156 4, 4, 0					
FFRB900	31x31	1.0		214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0				
FFRC900	31x31	1.0				214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0	
FFRB1156	35x35	1.0				214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0	
FFRC1156	35x35	1.0			214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0		
FFRB1517	40x40	1.0							214, 72, 572 4, 16, 0
FFRC1760	42.5x42.5	1.0					214, 96, 416 4, 32, 16		214, 96, 416 4, 32, 16

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence.
3. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
4. These packages are only offered in 0.8 mm ballpitch. All other packages are offered in 1.0 mm ball pitch.
5. GTH transceivers in the C784 package support data rates up to 12.5 Gb/s.

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AMD Zynq™ 7000 XQ FPGA Resources

		Device Name	XQ7Z020	XQ7Z030	XQ7Z045	XQ7Z100
Processing System (PS)		Processor Core	Dual-Core Arm® Cortex-A9 MPCore Up to 766 MHz	Dual-Core Arm Cortex-A9 MPCore Up to 800 MHz		
		Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor			
		L1 Cache	32 KB Instruction, 32 KB Data per processor			
		L2 Cache	512 KB			
		On-Chip Memory	256 KB			
		External Memory Support	DDR3, DDR3L, DDR2, LPDDR2			
		External Static Memory Support	2x Quad-SPI, NAND, NOR			
		DMA Channels	8 (4 Dedicated to PL)			
		Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
		Peripherals w/ built-in DMA	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO			
		Security(1)	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot			
		PS to PL Interface	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory, AXI 64b ACP, 16 Interrupts			
Programmable Logic (PL)		7 Series PL Equivalent	Artix™ 7	Kintex™ 7	Kintex 7	Kintex 7
		Logic Cells	85K	125K	350K	444K
		Look-Up Tables (LUTs)	53,200	78,600	218,600	277,400
		Flip-Flops	106,400	157,200	437,200	554,800
		Total Block RAM (# 36 Kb Blocks)	4.9Mb (140)	9.3Mb (265)	19.2Mb (545)	26.5Mb (755)
		DSP Slices	220	400	900	2,020
		PCI Express®	—	Gen2 x4	Gen2 x8	Gen2 x8
		Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs			
		Security(1)	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config			
	Speed Grades	Q-Temperature	-1	-1		–
		I-Temperature	-1, -2, -1L	-1, -2, -2L		-1, -2, -2L

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AMD Zynq™ 7000 XQ FPGA Packaging

Package [1]	Dimensions (mm)	Ball Pitch (mm)	XQZ7020	XQZ7030	XQZ7045	XQZ7100
			HRIO, HPIO PSIO[2], GTP 6.2Gb/s	HRIO, HPIO PSIO[2], GTX 10.3Gb/s		
CL400	17x17	0.8	125, 0 128, 0			
CL484	19x19	0.8	200, 0 128, 0			
RB484	23x23	1.0		100, 63 128, 4		
RF676[1]	27x27	1.0		100, 150 128, 4	100, 150 128, 8	
RFG676[1]	27x27	1.0			100, 150 128, 8	
RF900	31x31	1.0			212, 150 128, 16	212, 150 128, 16
RF1156	35x35	1.0				250, 150 128, 16

1. Devices in the same package are footprint compatible. FBG676 and FFG676 are also footprint compatible.
2. PS I/O count does not include dedicated DDR calibration pins.
3. PS DDR and PS MIO pin count is limited by package size. See DS196, *XQ Zynq-7000 All Programmable SoC Overview* for details.

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AMD Virtex™ and Kintex™ UltraScale+™ XQ FPGAs

	Device Name	XQKU5P	XQKU15P	XQVU3P	XQVU7P	XQVU11P
Logic	System Logic Cells (K)	475	1,143	862	1,724	2,835
	CLB Flip-Flops (K)	434	1,045	788	1,576	2,592
	CLB LUTs (K)	217	523	394	788	1,296
Memory	Max. Distributed RAM (Mb)	6.1	9.8	12.0	24.1	36.2
	Total Block RAM (Mb)	16.9	34.6	25.3	50.6	70.9
	UltraRAM (Mb)	18.0	36.0	90.0	180.0	270.0
Clocking	Clock Mgmt Tiles (CMTs)	4	11	10	20	12
Integrated IP	DSP Slices	1,824	1,968	2,280	4,560	9,216
	Peak INT8 DSP (TOPs)	–	–	7.1	14.2	28.7
	PCIe® Gen3 x16	1	5	2	4	3
	150G Interlaken	0	4	3	6	6
	100G Ethernet w/RS-FEC	1	4	3	6	9
I/O	Max. Single-Ended HD I/Os	96	96	–	–	–
	Max. Single-Ended HP I/Os	208	468	520	832	416
	GTH 16.3 Gb/s Transceivers	0	32	–	–	–
	GTY 28.2 Gb/s Transceivers	16	24	40	76	96
Speed Grades	M-Temperature	-1	-1	-1	–	–
	I-Temperature	-1 -1L -2	-1 -1L -2	-1 -2	-1 -2	-1 -2

Package[2]	Dimensions (mm)	Ball Pitch (mm)	HDIO, HPIO, GTH 16.3 Gb/s, GTY 28.2 Gb/s		HPIO, GTY 28.2 Gb/s		
SFRB784[3]	23x23	0.8	96, 208, 0, 16				
FFRB676	27x27	1.0	72, 208, 0, 16				
FRA1156[3]	35x35	1.0		48, 468, 20, 8			
FFRE1517	40x40	1.0		96, 416, 32, 24			
FFRC1517	40x40	1.0			520, 40		
FLRA2104	47.5x47.5	1.0				832, 52	
FLRB2104	47.5x47.5	1.0				702, 76	
FLRC2104	47.5x47.5	1.0					416, 96

Notes:

1. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
2. For full part number details, see the Ordering Information section in DS895, XQ *UltraScale Architecture* Overview.
3. GTY transceiver line rates are package limited: B784 to 12.5 Gb/s, and A1156 to 16.3 Gb/s. Refer to data sheet for details.

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AMD Kintex™ UltraScale™ XQ FPGAs

	Device Name	XQKU040	XQKU060	XQKU095	XQKU115
Logic Resources	System Logic Cells (K)	530	726	1,176	1,451
	CLB Flip-Flops	484,800	663,360	1,075,200	1,326,720
	CLB LUTs	242,400	331,680	537,600	663,360
Memory Resources	Maximum Distributed RAM (Kb)	7,050	9,180	4,800	18,360
	Block RAM/FIFO w/ECC (36 Kb each)	600	1,080	1,680	2,160
	Block RAM/FIFO (18 Kb each)	1,200	2,160	3,360	4,320
	Total Block RAM (Mb)	21.1	38.0	59.1	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	10	12	16	24
	I/O DLL	40	48	64	64
I/O Resources	Maximum Single-Ended HP I/Os	416	416	468	624
	Maximum Single-Ended HR I/Os	104	104	52	104
Integrated IP Resources	DSP Slices	1,920	2,760	768	5,520
	System Monitor	1	1	1	2
	PCIe® Gen1/2/3	3	3	4	6
	Interlaken	0	0	2	0
	100G Ethernet	0	0	2	0
	16.3 Gb/s Transceivers (GTH/GTY)	20	28	28[1]	64
Speed Grades	M-Temperature	-1	-1	-1	–
	I-Temperature	-1 -1L -2	-1 -1L -2	-1 -2	-1 -1L -2

Package[2, 3, 4, 5]	Dimensions (mm)	Ball Pitch (mm)	HRIO, HPIO, GTH/GTY			
RBA676[6]	27x27	1.0	104, 208, 16			
RFA1156	35x35	1.0	104, 416, 20	104, 416, 28	52, 468, 28	
RLD1517	40x40	1.0				104, 234, 64
RLF1924	45x45	1.0				104, 624, 64

Notes:
1. GTY transceivers in KU095 devices support data rates up to 16.3 Gb/s.
2. Packages with the same package footprint designator, e.g., A2104, are footprint compatible within XC and XQ UltraScale and UltraScale+ devices.
3. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
4. For full part number details, see the Ordering Information section in DS895, XQ *UltraScale Architecture* Overview.
5. See UG575, *UltraScale Architecture Packaging and Pinouts User Guide* for more information.
6. GTH transceivers in A676 packages support data rates up to 12.5 Gb/s.

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AMD Virtex™ 7 XQ FPGAs

	Device Name	XQ7V585T	XQ7VX330T	XQ7VX485T	XQ7VX690T	XQ7VX980T
Logic Resources	Slices	91,050	51,000	75,900	108,300	153,000
	Logic Cells	582,720	326,400	485,760	693,120	979,200
	CLB Flip-Flops	728,400	408,000	607,200	866,400	1,224,000
Memory Resources	Maximum Distributed RAM (Kb)	6,938	4,388	8,175	10,888	13,838
	Block RAM/FIFO w/ ECC (36 Kb each)	795	750	1,030	1,470	1,500
	Total Block RAM (Kb)	28,620	27,000	37,080	52,920	54,000
Clocking	CMTs (1 MMCM + 1 PLL)	18	14	14	20	18
I/O Resources	Maximum Single-Ended I/O	850	700	700	1,000	900
	Maximum Differential I/O Pairs	408	336	336	480	432
Integrated IP Resources	DSP Slices	1,260	1,120	2,800	3,600	3,600
	PCIe® Gen2[2]	3	—	4	—	—
	PCIe Gen3	—	2	—	3	3
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1
	GTX Transceivers (10.3 Gb/s Max Rate)[3]	36	—	28	—	—
	GTH Transceivers (11.3 Gb/s Max Rate)[4]	—	28	—	48	24
Speed Grades	M-Temperature	-1	-1	-1	—	—
	I-Temperature	-1, -2	-1, -2	-1, -2	-1, -2	-1
	E-Temperature	-2L	-2L	-2L	-2L	-2L

Package[1][5]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O:** HRIO, HPIO, GTX 10.3 Gb/s, GTH 11.3 Gb/s				
RF1157	35 x 35	1.0	0, 600, 20, 0	0, 600, 0, 20		0, 600, 0, 20	
RF1158	35 x 35	1.0				0, 350, 0, 48	
RF1761	42.5 x 42.5	1.0	100, 750, 36, 0	50, 650, 0, 28	0, 700, 28, 0	0, 850, 0, 36	
RF1930	45 x 45	1.0			0, 700, 24, 0	0, 1000, 0, 24	0, 900, 0, 24

Notes:
1. See DS185, *Defense-Grade 7 Series FPGAs Overview,* for package details. Other packages available with leaded external balls, see DS180: *7 Series FPGAs Overview* for XC package details.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
3. 10.3125 Gb/s support in -2 speed grade.
4. 11.3 Gb/s support in -2 speed grade.
5. RF#### packages are pin compatible with FF#### packages, for same/equivalent ####; see product pinout specifications for details about compatibility.

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AMD Kintex™ 7 XQ FPGAs

	Device Name	XQ7K325T	XQ7K410T
Logic Resources	Slices	50,950	63,550
	Logic Cells	326,080	406,720
	CLB Flip-Flops	407,600	508,400
Memory Resources	Maximum Distributed RAM (Kb)	4,000	5,663
	Block RAM/FIFO w/ ECC (36 Kb each)	445	795
	Total Block RAM (Kb)	16,020	28,620
Clock Resources	CMTs (1 MMCM + 1 PLL)	10	10
I/O Resources	Maximum Single-Ended I/O	500	500
	Maximum Differential I/O Pairs	240	240
Integrated IP Resources	DSP48 Slices	840	1,540
	PCIe® Gen2[2]	1	1
	Analog Mixed Signal (AMS) / XADC	1	1
	Configuration AES / HMAC Blocks	1	1
	GTX Transceivers (10.3 Gb/s Max Rate)	16	16
Speed Grades	M-Temperature	-1, -1L	-1
	I-Temperature	-1, -2, -2L	-1, -2, -2L
	E-Temperature	-2L	-2L

Package[1]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: HRIO, HPIO, GTX 10.3Gb/s	
RF676[3]	27 x 27	1.0	250, 150, 8	250, 150, 8
RF900[3]	31 x 31	1.0	350, 150, 16	350, 150, 16

Notes:
1. See DS185, *Defense-Grade 7 Series FPGAs Overview,* for package details.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
3. RF676 is footprint compatible with FFG676, and RF900 is footprint compatible with FFG900.

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AMD Artix™ 7 XQ FPGAs

	Device Name	XQ7A50T	XQ7A100T	XQ7A200T
Logic Resources	Logic Cells	52,160	101,440	215,360
	Slices	8,150	15,850	33,650
	CLB Flip-Flops	65,200	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	600	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	75	135	365
	Total Block RAM (Kb)	2,700	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	5	6	10
I/O Resources	Maximum Single-Ended I/O	250	300	500
	Maximum Differential I/O Pairs	120	144	240
Embedded Hard IP Resources	DSP Slices	120	240	740
	PCIe® Gen2[1]	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1
	Configuration AES / HMAC Blocks	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	4	8	8
Speed Grades	M-Temperature	-1	-1	-1
	I-Temperature	-1, -1L, -2	-1, -1L, -2	-1, -1L, -2

Package[3]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: HRIO, GTP 6.6 Gb/s		
CS324[4][7]	15 x 15	0.8		210, 0	
CS325[4][7]	15 x 15	0.8	150, 4		
RS484[4][7]	19 x 19	0.8			285, 4
FG484[5]	23 x 23	1.0	250, 4	285, 4	
RB484[5]	23 x 23	1.0			285, 4
RB676[6]	27 x 27	1.0			400, 8

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers. See the Package section of this table for details.
3. Other packages are available with leaded external balls, see DS180, *7 Series FPGAs Overview* for XC package details.
4. Devices in CS324 are footprint compatible with CSG324, similarly CS325 is compatible with CSG325, and RS484 is compatible with SBG484.
5. Devices in FGG484, FBG484, FG484, and RB484 are footprint compatible.
6. Devices in FGG676, FBG676, and RB676 are footprint compatible.
7. Devices in CS324, CS325, and RS484 packages are 0.8 mm ball pitch; all others are 1 mm ball pitch.

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Device Ordering Information

Versal™ XQ Adaptive SoCs

Device Name					Device Attributes				Package Definition			
XQ	2	V	E	3558	-1	M	S	E	S	B	V	A1444
Device Grade XC: Commercial XA: Automotive XQ: Defense	**Generation**(1) 2: Gen 2	**Architecture** Versal	**Series Name** E: AI Edge C: AI Core M: Prime P: Premium H: HBM R: RF	**Device Number** Digits 1-3: Value Identifier Digit 4: # of Primary Cores	**Speed Grade** -1: Slowest -2: Mid -3: Highest	**Voltage** L: Low M: Mid H: High	**Static Screen** S: Standard L: Low Static	**Temp Grade** E: 0 to 110°C(2) I: –40 to 110°C(2) Q: –40 to +125°C M: –55 to +125°C	**Ball Pitch** V: 0.92 mm, w/LSC N: 0.92 mm, no LSC S: 0.8 mm L: 1.0 mm	**Lid** S: Lidless, w/Stiffener Ring F: Lidded B: Lidless, no Stiffener Ring H: Lidded Overhang I: Lidless, w/Stiffener Ring & Overhang	**RoHS6 Code** (3) V: Pb-free Ball Q: Eutectic Ball R: Ruggedized, Eutectic Ball	**Footprint**

1. This character is only present in second generation Versal devices.
2. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime—except -1E and -3E (standard 0–100°C).
3. All packages have Pb-free bumps.

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Device Ordering Information

Zynq™ UltraScale+™ XQ RFSoC

XQ	ZU	##	DR	-1	F	F	R	D	####	M
Defense Grade	Zynq™ Ultrascale+™	Value Index	SoC Type DR: Quad APU Dual RPU RF Feature-set	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power -3: Fastest	F: Flip-Chip w/ 1.0 mm Ball Pitch	F: Lid S: Lidless Stiffener	R: Ruggedized Package Q: Sn/Pb balls Pb-free inside	Package Designator	Package Pin Count	Temperature Grade (I,M)

Zynq™ UltraScale+™ XQ MPSoC

XQ	ZU	#	EV	-1	F	F	R	A	####	M
Defense Grade	Zynq™ Ultrascale+™	Value Index	SoC Type CG: Dual APU Dual RPU EG: Quad APU Dual RPU Single GPU EV: Quad APU Dual RPU Single GPU Single VCU	Speed Grade -1: Slowest -L1: Low Power -2: Mid -3: Fastest	F: Flip-Chip w/ 1.0 mm Ball Pitch S: Flip-Chip w/ 0.8 mm Ball Pitch	F: Lid B: Lidless	R: Ruggedized Package Q: Sn/Pb balls Pb-free inside	Package Designator	Package Pin Count	Temperature Grade (I,M)

Zynq™ 7000 XQ SoC

XQ	7	Z	###	-1	RF	###	Q
Defense Grade	7 Series	Zynq™	Value Index	Speed Grade -1: Slowest -L1: Low Power -1 -2: Mid -L2: Fastest -2	CL: Standard Lid Pb internal & external Flip-Chip w/ 0.8 mm ball pitch RB: Ruggedized Lid Flip-Chip w/ 1.0 mm ball pitch RF: Ruggedized Lid Flip-Chip w/ 1.0 mm ball pitch	Nominal Package Pin Count	Temperature Grade (I,Q)

M = Military (Tj = -55°C to +125°C)
Q = Automotive (Tj= -40°C to +125°C)
I = Industrial (Tj = -40°C to +100°C)

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Device Ordering Information

Kintex™ UltraScale+™ XQ
Virtex™ UltraScale+ XQ

XQ	V	U	#	P	-1	F	L	R	A	#	M
Defense Grade	V: Virtex K: Kintex	UltraScale	Value Index	Denotes UltraScale+	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power -3: Fastest	F: Flip-Chip w/ 1.0 mm Ball Pitch S: Flip-Chip w/ 0.8 mm Ball Pitch	F: Lid L: Lid SSI B: Lidless S: Lidless SSI Stiffener H: Lid Overhang SSI I: Lidless Overhang SSI Stiffener	R: Ruggedized Package Q: Sn/Pb balls Pb-free inside	Footprint Alpha	Package Pin Count	Temperature Grade (I,M)

Kintex UltraScale™ XQ

XQ	K	U	###	-1	RF	A	####	M
Defense Grade	K: Kintex	UltraScale	Value Index	Speed Grade -1: Slowest -L1: Low Power -2: Mid	RB: Ruggedized Lid Flip-Chip w/ 0.8 mm ball pitch RF: Ruggedized Lid Flip-Chip w/ 1.0 mm ball pitch RL: Ruggedized SSI Lid Flip-Chip w/ 1.0 mm ball pitch	Footprint Alpha	Package Pin Count	Temperature Grade (I,M)

M = Military (Tj = -55°C to +125°C)
I = Industrial (Tj = -40°C to +100°C)

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Device Ordering Information

Artix™ 7 XQ
Kintex™ 7 XQ
Virtex™ 7 XQ

XQ	7	A	###	-1	RF	###	M
Defense Grade	7 Series	A: Artix K: Kintex V: Virtex	Value Index	Speed Grade -1: Slowest -L1: Low Power -1 -2: Mid -L2: Low Power -2	CS: Standard Lid Pb internal & external Wire-bond Chip-Scale w/ 0.8 mm ball pitch FG: Standard Lid Pb internal & external (for XQ) Flip-Chip w/ 1.0 mm ball pitch RB: Ruggedized Lid Flip-Chip w/ 1.0 mm ball pitch RS: Ruggedized Lid Flip-Chip w/ 0.8 mm ball pitch RF: Ruggedized Lid Flip-Chip w/ 1.0 mm ball pitch	Nominal Package Pin Count	Temperature Grade (M, I, E)

M = Military (Tj = -55°C to +125°C)
I = Industrial (Tj = -40°C to +100°C)
E = Extended (Tj= 0°C to +100°C)

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