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Automotive-Grade AMD Versal XA Adaptive SoC Overview

	AMD Versal™ AI Edge XA Series
Application Processor	Dual-core Arm Cortex-A72 up to 18.4k DMIPS
Real-Time Processor	Dual-core Arm Cortex-R5F up to 2,672 DMIPS
AI Engine-ML Tiles	8–304 Tiles / 5–202 INT8 TOPS
External Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, w/ ECC
Programmable Logic	44k – 1.1M System Logic Cells
DSP Slices	90 – 1,312
Speed Grades	-1
Automotive Standards	AEC-Q100, Production Part Approval Process
Power Management	Separate Voltage on PS & PL, with Overall System Power (FPD + LPD + PL) Full Power Domain / Low Power Domain / Programmable Logic Power Domain / Platform Management Controller (PMC)

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Automotive-Grade AMD Zynq SoC Comparison

	AMD Zynq™ UltraScale+™ XA MPSoC	Zynq 7000 XA SoC
Application Processor	Quad-core Arm® Cortex®-A53 MPCore™ up to 1.2 GHz	Dual-core Arm Cortex-A9 MPCore up to 667 MHz
Real-Time Processor	Dual-core Arm Cortex-R5 MPCore up to 500 MHz	N/A
AI Engine-ML Tiles	Mali™-400 MP2 up to 600 MHz	N/A
External Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC	x16/x32: DDR3L, DDR3, DDR2, LPDDR2 w/ECC (supports 16-bit)
Programmable Logic	103K–653 System Logic Cells	28K–125K Logic Cells
DSP Slices	240–2,928	80–400
Speed Grades	-1, -1L(1)	-1
Automotive Standards	AEC-Q100, Production Part Approval Process, ISO 26262, IEC 61508, and ISO 13849 certified	AEC-Q100, Production Part Approval Process, ISO 26262, IEC 61508, and ISO 13849 certified
Power Management	Separate Voltage on PS & PL, with Overall System Power (FPD + LPD + PL)/ Full Power Domain / Low Power Domain/ Programmable Logic Power Domain	Overall System Power (FPD + LPD + PL) Separate Voltage on PS & PL

Notes: 1. ZU11EG and ZU7EV -1L speed grades are not supported.

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Automotive-Grade FPGA Device Comparison

	AMD Artix™ 7 XA	AMD Kintex™ 7 XA	AMD Spartan™ 7 XA	AMD Artix UltraScale+™ XA	AMD Spartan UltraScale+™ XA
Core Voltage	1.0V	1.0V	1.0V	1.2V	1.0V
Logic Cells	12K–101K	162K	6K–102K	82K–170K	36k
Total Block RAM (K)	720–4,860	2,188	180–4,320	3,600-5,100	1,728
CMTs	3–6	8	2–8	3	2
DSP Slices	40–240	600	10–160	216–576	48
PCI Express®	1 x Gen2x4	1 x Gen2x8	~~0~~	1 x Gen3x8 1 x Gen4x8	0
Serial Transceivers	2–4	8	0	12	0
Speed Grades	-1, -2	-1	-1, -2	-1, -1L	-1, -1L
Automotive Standards	AEC-Q100, Production Part Approval Process	AEC-Q100, Production Part Approval Process	AEC-Q100, Production Part Approval Process	AEC-Q100, Production Part Approval Process	AEC-Q100, Production Part Approval Process

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AMD Versal™ AI Edge XA Series Resources

	Device Name[1]	XAVE2002	XAVE2102	XAVE2202	XAVE2302	XAVE1752	XAVE2602	XAVE2802
Intelligent Engines	AI Engine-ML Tiles	8	12	24	34	0	152	304
	AI Engine Tiles	0	0	0	0	304	0	0
	AIE/AIE-ML Data Memory (Mb)	4	6	12	17	76	76	152
	AIE-ML Shared Memory (Mb)	48	48	68	68	0	304	304
	DSP Engines	90	176	324	464	1,312	984	1,312
Adaptable Engines	System Logic Cells	43,750	80,080	229,688	328,720	981,120	820,313	1,139,040
	LUTs	20,000	36,608	105,000	150,272	448,512	375,000	520,704
	NoC Master / NoC Slave Ports	2	2	5	5	21	21	21
	Distributed RAM (Mb)	0.6	1.1	3.2	4.6	13.7	11.4	15.9
	Block RAM Blocks	24	47	108	155	954	476	600
Memory	Total Block RAM (Mb)	0.8	1.7	3.8	5.4	33.5	16.7	21.1
	UltraRAM Blocks	24	47	108	155	462	224	264
	UltraRAM (Mb)	6.8	13.2	30.4	43.6	129.9	63.0	74.3
	Accelerator RAM (Mb)	32	32	32	32	0	0	0
	Total PL Memory (Mb)	40.2	48	69.4	85.6	177.1	91.1	111.3
	DDR Memory Controllers	1	1	1	1	3	3	3
	DDR Bus Width	64	64	64	64	192	192	192
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex-A72, 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC						
	Real-Time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC						
	Memory	256KB On-Chip Memory w/ECC						
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)						
Serial Transceivers	GTY Transceivers	0	0	0	0	44	0	0
	GTYP Transceivers	0	0	8	8	0	32[1]	32[1]
Integrated Protocol IP	PCIe® w/DMA (CPM)		-	-	-	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16
	PCI Express®		-	1 x Gen4x8	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8
	40G Multirate Ethernet MAC		0	1	1	2	2	2
	Video Decoder Engines (VDEs)		–	–	–	–	2	4
	Platform Mgmt Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug						
Speed Grades	I-Grade	-1LSI (0.725V), -1LLI (0.725V)						
	Q-Grade	-1LLQ (0.725V), -1LSQ (0.725V)						

1. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.

Important: Verify all data in this document with the device data sheets.

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AMD Versal™ AI Edge XA Series – Packaging

			XAVE2002	XAVE2102	XAVE2202	XAVE2302	XAVE1752	XAVE2602	XAVE2802
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTY, GTYP						
SBVA484	19x19	0.8	108, 0, 54 0, 78 0, 0	108, 0, 54 0, 78 0, 0					
SBVA625	21x21	0.8	132, 30, 54 0, 78 0, 0	132, 30, 54 0, 78 0, 0					
SFVA784	23x23	0.8	132, 30, 54 0, 78 0, 0	132, 30, 54 0, 78 0, 0	132, 30, 54 22, 78 0, 8	132, 30, 54 22, 78 0, 8			
NSVG1369	35x35	0.92					132, 246, 0 44, 78 24, 0		
NSVH1369	35x35	0.92						132, 192, 0 44, 78 0, 32	132, 192, 0 44, 78 0, 32
VSVA1596	37.5x37.5	0.92					192, 186, 0 44, 78 32, 0		
VSVH1760	40x40	0.92						186, 300, 0 44, 78 0, 32	186, 300, 0 44, 78 0, 32
VSVA2197	45x45	0.92					192, 294, 0 44, 78 44, 0		

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AMD Zynq™ UltraScale+™ XA MPSoCs Resources

		Device Name[1]	XAZU1EG	XAZU2EG	XAZU3EG	XAZU3TEG	XAZU11EG	XAZU4EV	XAZU5EV	XAZU7EV
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.2 GHz							
		Memory w/ECC	L1 Cache 32 KB I / D per core, L2 Cache 1 MB, on-chip Memory 256 KB							
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5 MPCore up to 500 MHz							
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128 KB per core							
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 600 MHz							
		Memory	L2 Cache 64 KB							
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC							
		Static Memory Interfaces	NAND, 2x Quad-SPI							
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet							
		General Connectivity	2xUSB 2.0, 2x SD/SDIO/eMMC, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO							
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains							
		Security	RSA, AES, and SHA							
		AMS - System Monitor	10-bit, 1 MSPS - Temperature, Voltage, and Current Monitor							
PS to PL Interface			12 x 32/64/128b AXI Ports							
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	81	103	154	157	653	192	256	504
		CLB Flip-Flops (K)	74	94	141	144	597	176	234	461
		CLB LUTs (K)	37	47	71	72	299	88	117	230
	Memory	Max. Distributed RAM (Mb)	1.0	1.2	1.8	2.1	9.1	2.6	3.5	6.2
		Block RAM Blocks	108	150	216	144	600	128	144	312
		Total Block RAM (Mb)	3.8	5.3	7.6	5.1	21.1	4.5	5.1	11.0
		Ultra RAM Blocks	-	-	-	48	80	48	64	96
		Ultra RAM (Mb)	-	-	-	14	22.5	13.5	18.0	27.0
	Clocking	Clock Management Tiles (CMTs)	3	3	3	1	8	4	4	8
	Integrated IP	DSP Slices	216	240	360	576	2928	728	1,248	1,728
		VCU	-	-	-		-	1	1	1
		PCI Express®	–	–	–	1 x Gen3x8	2 x Gen3x16	2 x Gen3x8[1]	2 x Gen3x8[1]	2 x Gen3x8[1]
		AMS - System Monitor	1	1	1	2	1	1	1	1
	Transceivers	GTH 12.5 Gb/s Transceivers	-	-	-	8	32	16	16	16
	Speed Grades	I-Grade[2]	-1 (0.85V), -L1 (0.72V)			-1 (0.85V), -L1 (0.72V/0.85V)	-1 (0.85V)	-1 (0.85V), -L1 (0.72V)		-1 (0.85V)
		Q-Grade	-1 (0.85V)					-1 (0.85V)		

1. Gen3x16 is also supported.

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AMD Zynq™ UltraScale+™ XA MPSoCs Packaging

PS I/Os(1), 3.3V High-Density (HD) I/O, 1.8V High-Performance (HP) I/Os
PS-GTR 6 Gb/s, GTH 12.5 Gb/s

Pkg Footprint(2)	Dimensions (mm)	Ball Pitch (mm)	XAZU1EG	XAZU2EG	XAZU3EG	XAZU3TEG	XAZU11EG	XAZU4EV	XAZU5EV	XAZU7EV
SBVA484	19x19	0.8	170, 24, 58 4, 0	170, 24, 58 4, 0	170, 24, 58 4, 0					
SFVA625	21x21	0.8	170, 24, 156 4, 0	170, 24, 156 4, 0	170, 24, 156 4, 0					
SFVC784	23x23	0.8	214, 24, 156 4, 0	214, 96, 156 4, 0	214, 96, 156 4, 0	214, 72, 52 4, 4		214, 96, 156 4, 4	214, 96, 156 4, 4	
SFVD784	23x23	0.8				214, 72, 52 4, 8				
FBVB900	31x31	0.8								214, 48, 156 4, 16
FFVF1517	40x40	1.0					214, 48, 416 4, 32			

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

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AMD Zynq™ 7000 XA SoCs Resources & Packaging

		Device Name[1]		XA7Z010	XA7Z020	XA7Z030
Processing System (PS)	Application Processor Unit	Processor Core		**Dual** Arm® Cortex®-A9 MPCore™ up to 667 MHz		
		Processor Extension		NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per Processor		
	Memory	L1 Cache		32 KB I / D per Core		
		L2 Cache		512 KB		
		On-Chip Memory		256 KB		
	External Memory	Dynamic Memory Interface		x32/x64: DDR3, DDR3L, DDR2, LPDDR2		
		Static Memory Interfaces		NAND, NOR, 2x Quad-SPI		
	Connectivity	High-Speed Connectivity		2x Tri-mode Gigabit Ethernet		
		General Connectivity		2xUSB 2.0, 2x SD/SDIO/eMMC, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Integrated Block Functionality	Security		RSA, AES, and SHA		
		AMS - System Monitor		2x12-bit, 1 MSPS - Temperature, Voltage, and Current Monitor		
PS to PL Interface				9 x 32/64 AXI Ports		
Programmable Logic (PL)	Programmable Functionality	7 Series PL Equivalent		Artix 7	Artix 7	Kintex 7
		Logic Cells		28,160	85,280	125,760
		CLB Flip-Flops		35,300	106,400	157,200
		CLB LUTs		17,600	53,300	78,600
	Memory	Total Block RAM (KB) (# 36 Kb Blocks)		240 (60)	560 (140)	1,060 (265)
	Integrated IP	DSP Slices		80	220	400
		Peak DSP Performance		100 GMACs	276 GMACs	593 GMACs
		PCI Express®		-	-	Gen2 x4
		AMS / XADC		AES and SHA 256b Decryption and Authentication for Secure Programmable Configuration		
	Speed Grades	I-Grade		-1		
		Q-Grade		-1		
				HR I/O[2], HP I/O[3], PS I/O[4], GTX Transceiver		
Package[1]	CLG225	13x13	0.8	54, 0, 84, 0		
	CLG400	17x17	0.8	100, 0, 128, 0	125, 0, 128, 0	
	CLG484	19x19	0.8		200, 0, 128, 0	
	FBV484	23x23	1.0			100, 63, 128, 4

Notes:
1. All packages listed are Pb-free.
2. HR = High Range I/O with support for I/O voltage from 1.2V up to 3.3V.
3. HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.
4. PS I/O includes user I/O and DDR I/O.

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AMD Artix™ UltraScale+™ XA Resources & Packaging

	Device Name	XAAU7P	XAAU10P	XAAU15P
Logic Resources	System Logic Cells	81,900	96,250	170,625
	CLB Flip-Flops	74,880	88,000	156,000
	CLB LUTs	37,440	44,000	78,000
Memory Resources	Maximum Distributed RAM (Kb)	1.1	1.0	2.5
	Block RAM (36 Kb each)	108	100	144
	Total Block RAM (Kb)	3,888	3,600	5,184
Clock Resources	Clock Management Tiles (CMTs)	2	3	3
I/O Resources	HDIO	144	72	72
	HPIO	104	156	156
Embedded Hard IP Resources	DSP Slices	216	400	576
	PCI Express®	1x Gen3x4	1x Gen4x8	1x Gen4x8
	Analog Mixed Signal (AMS) / XADC	1	1	1
	GT @ 12.5 Gb/s or 16 Gb/s[1]	4	12	12
Speed Grades	I-Grade	-1,-1L	-1,-1L	-1,-1L
	Q-Grade	-1	-1	-1

Package	Dimensions (mm)	Ball Pitch (mm)	HD I/O, HP I/O, GTH, GTY		
FCVA289	9 x 9	0.5	72, 58, 4, 0		
FFVB676	27 x 27	1.0		72, 156, 12, 0	72, 156, 12, 0
SBVB484	19 x 19	0.8		48, 156, 12, 0	48, 156, 12, 0
SBVC484	19 x 19	0.8	144, 104, 4, 0		

Notes:
1. GTH and GTY data rates are package dependent:
   - Maximum 12.5 Gb/s in SBVB484, SBVC484
   - Maximum 16.3 Gb/s in FFVB676

Important: Verify all data in this document with the device data sheets.

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AMD Artix™ 7 XA FPGAs Resources & Packaging

		Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)						
	Part Number	XA7A12T	XA7A15T	XA7A25T	XA7A35T	XA7A50T	XA7A75T	XA7A100T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400	600	892	1,188
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50	75	105	135
	Total Block RAM (Kb)	720	900	1,620	1,800	2,700	3,780	4,860
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	285	285
	Maximum Differential I/O Pairs	72	120	72	120	120	137	137
Embedded Hard IP Resources	DSP Slices	40	45	80	90	120	180	240
	PCI Express®[1]	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTP Transceivers (6.25 Gb/s Max Rate)[2]	2	4	4	4	4	4	4
Speed Grades	I-Grade	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Q-Grade	-1	-1	-1	-1	-1	-1	-1

Package[3]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)					
CPG236	10 x 10	0.5		106 (2)		106 (2)	106 (2)		
CPG238	10 x 10	0.5	112 (2)		112 (2)				
CSG324	15 x 15	0.8		210 (0)		210 (0)	210 (0)	210 (0)	210 (0)
CSG325	15 x 15	0.8	150 (2)	150 (4)	150 (4)	150 (4)	150 (4)		
FGG484	23 x 23	1.0						285 (4)	285 (4)

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the CSG324 devices are available without transceivers. See the Package section of this table for details.
3. Device migration is available within the Artix 7 family for like packages but is not supported between other 7 series families.

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Important: Verify all data in this document with the device data sheets.

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AMD Kintex™ 7 XA FPGAs

	Device Name	XA7K160T
Logic Resources	Logic Cells	162,240
	Slices	25,350
	CLB Flip-Flops	202,800
Memory Resources	Maximum Distributed RAM (Kb)	2,188
	Block RAM/FIFO w/ ECC (36 Kb each)	325
	Total Block RAM (Kb)	11,700
Clock Resources	CMTs (1 MMCM + 1 PLL)	8
I/O Resources	Maximum Single-Ended I/O	400
	Maximum Differential I/O Pairs	192
Embedded Hard IP Resources	DSP Slices	600
	PCI Express®(1)	1x Gen2x4
	Analog Mixed Signal (AMS) / XADC	1
	Configuration AES / HMAC Blocks	1
	GTX Transceivers (8.0 Gb/s Max Rate)(2)	8
Speed Grades	I-Grade	-1

Package(3)	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O, 1.8V HP 1/O, GTX Transceivers
FFG676	27 x 27	1.0	250, 150, 8

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available.
3. Device migration is not supported between other 7 series families.

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AMD Spartan™ UltraScale+™ XA Resources & Packaging

	Device Name	XASU35P
Logic Resources	System Logic Cells	35,700
	CLB Flip-Flops	32,640
	CLB LUTs	16,320
Memory Resources	Maximum Distributed RAM (Kb)	0.2
	Block RAM (Mb)	1.7
	Total Block RAM (Kb)	1,728
Clock Resources	Clock Management Tiles (CMTs)	2
I/O Resources	HDIO	252
	HPIO	52
Embedded Hard IP Resources	DSP Slices	48
	PCI Express®	0
Speed Grades	I-Grade	-1,-1L
	Q-Grade	-1

Package	Dimensions (mm)	Ball Pitch (mm)	HD I/O, HP I/O
CMVA529	12 x 12	0.8	252, 52

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AMD Spartan™ 7 XA FPGAs

Part Number			XA7S6	XA7S15	XA7S25	XA7S50	XA7S75	XA7S100
Logic Cells			6,000	12,800	23,360	52,160	76,800	102,400
Slices			938	2,000	3,650	8,151	12,000	16,000
CLB Flip-Flops			7,500	16,000	29,200	65,200	96,000	128,000
Max. Distributed RAM (Kb)			70	150	313	600	832	1,100
Block RAM/FIFO w/ ECC (36 Kb each)			5	10	45	75	90	120
Total Block RAM (Kb)			180	360	1,620	2,700	3,240	4,320
Clock Mgmt Tiles (1 MMCM + 1 PLL)			2	2	3	5	8	8
Max. Single-Ended I/O Pins			100	100	150	250	400	400
Max. Differential I/O Pairs			48	48	72	120	192	192
DSP Slices			10	20	80	120	140	160
Analog Mixed Signal (AMS) / XADC			0	0	1	1	1	1
Configuration AES / HMAC Blocks			0	0	1	1	1	1
I-Grade			-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2
Q-Grade			-1	-1	-1	-1	-1	-1
Package	Dimensions (mm)	Ball Pitch (mm)	Available User I/O: 3.3V SelectIO™ HR I/O					
CPGA196	8x8	0.5	100	100				
CSGA225	13x13	0.8	100	100	150			
CSGA324	15x15	0.8			150	210		
FGGA484	23x23	1.0				250	338	338
FGGA676	27x27	1.0					400	400

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Adaptive SoC Ordering Information

Versal™ AI Edge XA

XA	V	E	####	-1	L	S	I	S	S	V	A2112
Automotive Grade	Architecture	Series	Device Number Digits 1-3: Value Identifier Digit 4: # of Primary Cores	Speed Grade -1 = Standard	Voltage L: Low (0.7V)	Static Screen S: Standard L: Low Static	Temp Grade I: –40 to 110°C(1) Q: –40 to +125°C	Ball Pitch V: 0.92 mm, w/LSC N: 0.92 mm, no LSC S: 0.8 mm	Lid S: Lidless, w/Stiffener Ring F: Lidded B: Lidless, no Stiffener Ring	RoHS6 Code (2) V: Pb-free Ball	Footprint

Zynq™ UltraScale+™ XA

XA	ZU	#	E	G	-1	S	B	V	A	484	I
Automotive Grade	Family	Value Index(3)	Processor System E: Dual RPU Quad APU Single GPU	Engine Type G: General Purpose V: Video	Speed Grade -1 = Standard -1L = Low Power	S: Flip-Chip (.8 mm)	F: Lid B: Lidless	V: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (I, Q)

Zynq 7000 XA

XA	7	Z	#	-1	FB	V	484	Q
Automotive Grade	Generation	Family	Value Index	Speed Grade -1 = Standard	CL: Wire-bond (.8 mm) FB: Flip-Chip (1 mm)	V: RoHS 6/6 G: RoHS 6/6	Package Pin Count	Temperature Grade (I, Q)

I = Tj from –40°C to +100°C ; Q = Tj from –40°C to +125°C

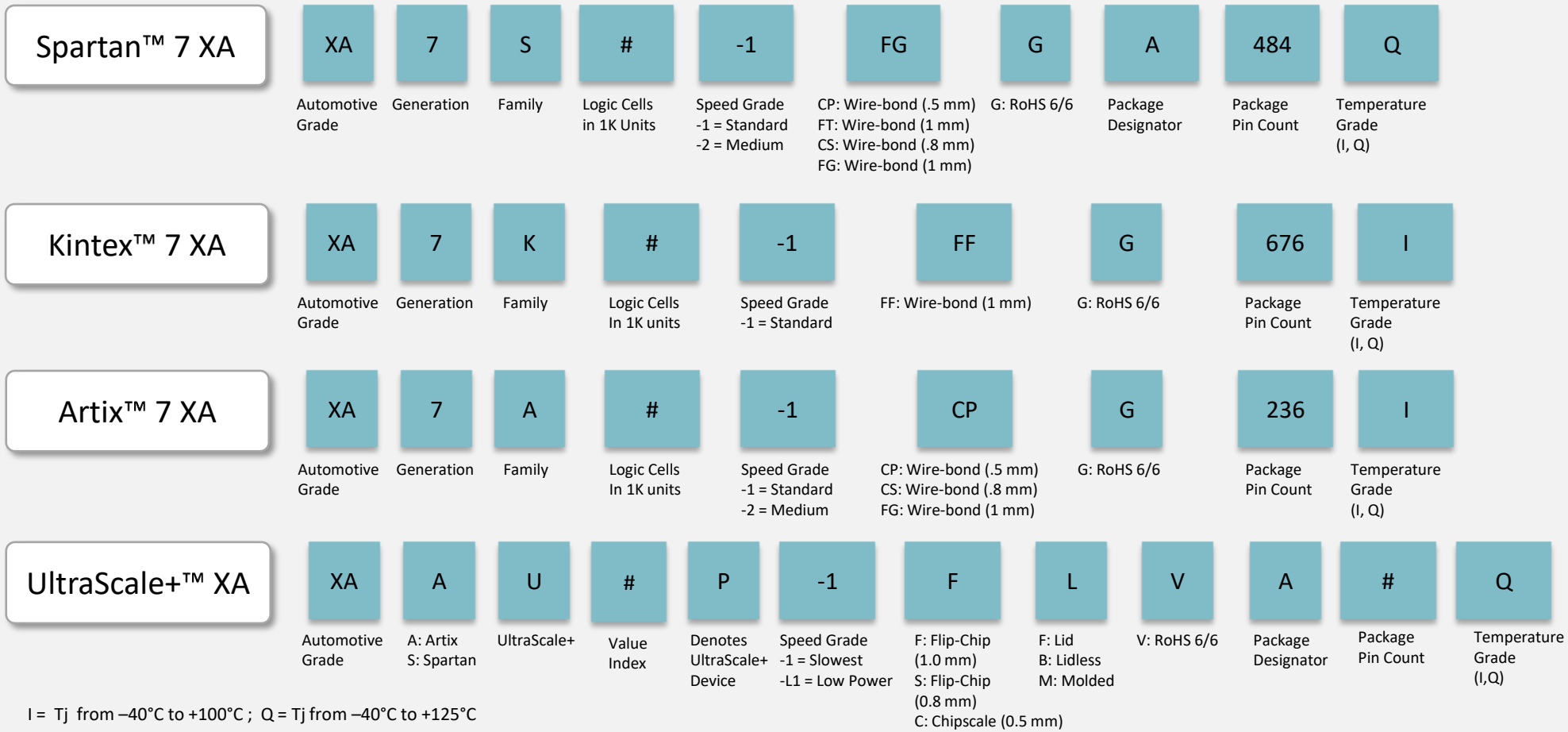
1. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime
2. All packages have Pb-free bumps.
3. T in XA ZU3T value index denotes increase in resources and transceivers vs. XAZU3

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Important: Verify all data in this document with the device data sheets.

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FPGA Ordering Information



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